Applicants respectfully submit that the subject matter of new claims 40-49 is fully supported in the specification as originally filed. No new matter has been introduced.

Claims 39 and 40 have been canceled without prejudice and without abandonment of the subject matter thereof. The claim language from canceled claims 39 and 40 has been added to independent claim 38.

Figure 9 stands objected to for failing to include reference numbers 120 and 122. Applicant respectfully points out that Figure 9 does in fact include reference numbers 120 and 122, so the objection to Figure 9 is believed to be overcome.

Figure 4 has been amended to include reference number 9. Applicant respectfully submits that the informal drawing of Figure 4 as originally filed included reference number 9, so no new matter is believed to be introduced.

The drawings stand objected to for failing to show the limitations in claims 14 and 26. With regard to claim 14, Applicant respectfully points out calibration circuitry 30 in Figure 7 has the same structure as the test circuitry in Figure 6 and the test circuitry 20 of Figure 5. Therefore, the drawings show the feature of claim 14. With regard to claim 26, Applicant adds language in the specification from the language appearing in claim 26. Applicant also adds new Figure 10 which shows an apparatus as described in claim 26. Because claim 26 appeared in the application as originally filed, no new matter is believed to

be introduced. The objection to the drawings concerning the limitations recited in claims 14 and 26 is believed to be overcome.

Claims 1-4, 7, 9-10, 14, 16-17, 19, 21-26, 28, 30-31 and 37-39 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Katakura U.S. Patent 6,044,034 (hereinafter "Katakura"). In response to the rejection, Applicant respectfully submits the following.

Initially, Applicant respectfully points out that claim 7 depends from objected-to claim 6 and is therefore believed to be merely objected to. In the same way, claims 9 and 10 are believed to be merely objected to for depending from objected-to claim 8; claim 14 is believed to be merely objected-to for depending from objected-to claim 13; claim 28 is believed to be merely objected-to for depending from objected-to claim 27; and claims 30 and 31 are believed to be merely objected to for depending from objected-to claim 29.

Claim 1 recites test circuitry, coupled to at least one bit line, for placing on an external pad of the integrated circuit chip a current level corresponding to a voltage level appearing on the at least one bit line, while concurrently disabling the sense amplifier circuitry. In contrast, Applicant respectfully submits that there is no test circuitry disclosed in Katakura.

Further, though sense amplifier circuitry 81 is shown as including an enable input, Katakura does not show sense amplifier circuitry 81 being disabled when a current level corresponding to a voltage level appearing on at least one bit line is placed on an

external pad, in contradiction with a statement made in the outstanding Office Action. In particular, the passage of Katakura relied upon in the Office Action (col. 2, lines 26-28) merely refers to the fact that any memory cell in the Katakura multi-port memory cannot be written to while being read from, from the group of data lines associated with the same memory port, and thus does not suggest that sense amplifiers are disabled when the Katakura multi-port memory is providing data from a read operation. In fact, Katakura seems to show that sense amplifiers are enabled when data is provided by the multi-port memory. In an absence of a showing or suggestion in Katakura of test circuitry, and particularly test circuitry as recited in claim 1, claim 1 and the claims that depend therefrom are believed to be allowable over Katakura.

Claim 16 has been amended to recite selecting a bit line while sense amplifier circuitry is disabled; and providing, while the sense amplifier circuitry coupled to the selected bit line remains disabled, a current level to a pad corresponding to a voltage level appearing on the selected bit line. Applicant respectfully submits that the memory device of Katakura is not believed to disable sense amplifier circuitry when a bit line is selected and/or when a current level corresponding to a voltage level of the selected bit line is provided to a pad. As stated above, sense amplifier circuitry 81 is enabled and not disabled during a read access operation in which data from addressed memory cells are provided externally to the Katakura memory device. Consequently, the

invention of claim 16 is not believed to be shown or suggested by Katakura, so claim 16 and the claims that depend therefrom are believed to be allowable.

Claim 22 has been amended to recite an apparatus test circuitry, coupled to at least one bit line for placing on an external pad during a test mode of operation a current level corresponding to a voltage level appearing on the at least one bit line, the sense amplifier circuitry, including sense amplifier circuitry coupled to the at least one bit line, being disabled during the test mode of operation. In contrast, Katakura fails to show test circuitry operable during a test mode of operation, much less test circuitry providing a current level as claimed while sense amplifier circuitry coupled to the at least one bit line is disabled. Again, the Katakura memory device enables sense amplifiers coupled to a selected bit line when data is provided externally to the Katakura memory device via the selected bit line. In an absence of any prior teaching or suggestion in Katakura of an apparatus as claimed, claim 22 and the claims that depend therefrom are believed to be allowable.

Claim 37 has been amended to recite an apparatus having means for placing a current, including a first transistor having a control terminal coupled to a plate of the ferroelectric capacitor, a first conduction terminal coupled to the external pad and a second conduction terminal connected to a voltage reference, and a second transistor having *a first conduction terminal connected to the external pad* and a second conduction terminal connected to

the first conduction terminal of the first transistor, and a means for *selectively activating the second transistor during the test mode of operation.* Applicant respectfully submits that the Katakura memory device does not show or suggest a test mode of operation, much less a means for selectively activating the second transistor during the test mode of operation. Instead, transistor 15B in the Katakura memory device is activated during normal operation when there is a memory read operation for read port B.

Further, transistor 15B is not *connected* to an external pad as claimed. Instead, transistor 15B is connected to data line RB.

As a result, it cannot be said that Katakura shows or suggests the invention of amended claim 22. Claim 22 is believed to be allowable.

New claims 40-49 depend from pending independent claims. Each new claim 40-49 is therefore believed to be allowable for at least the reason(s) presented above with respect to its corresponding independent claim.

For example, new claims 40-43 recite that the provided current level is proportional to a voltage level. Applicant respectfully submits that Katakura fails to show or suggest providing a current level that is proportional to a voltage level of a selected data line, or a current level that is proportional to a voltage level appearing across a capacitor. Claims 40-43 are believed to be allowable as a result.

Claim 45 recites a counter having an output coupled to the control terminal of the claimed second transistor. Clearly,

Katakura fails to show or suggest a counter as claimed. Claim 45 is believed to be allowable.

New claim 47 recites calibration circuitry. Katakura does not seem to show calibration circuitry whatsoever, in part because the Katakura memory device does not include test circuitry. Claim 47 and the claims that depend therefrom are believed to be allowable.

Marked up versions of the amended claims showing all the changes relative to the previous version of such claims appear above. Attached to the present Amendment as an appendix is a clean copy of the claims as amended. Further attached is an appendix of a clean version of the paragraph from the specification that has been amended.

In view of the above, it is believed that this application is in a condition for allowance, and such a Notice is respectfully requested.

Favorable consideration is respectfully requested.

Respectfully submitted,

JENKENS & GILCHRIST, P.C.

William F. Esser

Date: 6-10-03

William F. Esser
Reg. No. 38,053

Jenkens & Gilchrist
1445 Ross Avenue, Suite 3200
Dallas, Texas 75202-2799
214/855-4181
214/855-4300 (fax)

APPENDIX OF AMENDMENTS TO THE CLAIMS
Clean Version

16. (Amended) A method of testing a semiconductor memory device having an array of memory cells and sense amplifier circuitry coupled to bit lines of the array, the semiconductor memory device being in an integrated circuit chip, the method comprising:

connecting memory cells in a row of memory cells to bit lines of the array;

disabling the sense amplifier circuitry from driving the bit lines;

selecting a bit line while the sense amplifier circuitry remains disabled; and

providing a current level to a pad in the integrated circuit chip corresponding to a voltage level appearing on the selected bit line while the sense amplifier circuitry coupled to the selected bit line remains disabled.

22. (Amended) An apparatus, comprising:

a random access memory device, comprising:

a memory array of memory cells organized into rows and columns, including a plurality of word lines and bit lines, each row of memory cells being coupled to a word line and each column of memory cells being coupled to a bit line;

sense amplifier circuitry coupled to the bit lines;

address decode circuitry for receiving an address value and

asserting a row line associated therewith; and

test circuitry, coupled to at least one bit line for placing on an external pad during a test mode of operation a current level corresponding to a voltage level appearing on the at least one bit line, the sense amplifier circuitry, including sense amplifier circuitry coupled to the at least one bit line, being disabled during the test mode of operation.

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37. (Amended) An apparatus, comprising:

a ferroelectric capacitor; and

means for placing on an external pad of the apparatus during a test mode of operation a current level corresponding to a voltage level appearing across the ferroelectric capacitor, comprising a first transistor having a control terminal coupled to a plate of the ferroelectric capacitor, a first conduction terminal coupled to the external pad and a second conduction terminal connected to a voltage reference, and a second transistor having a first conduction terminal connected to the external pad and a second conduction terminal connected to the first conduction terminal of the first transistor, and a means for selectively activating the second transistor during the test mode of operation.

APPENDIX OF AMENDMENTS TO THE SPECIFICATION
Clean Version

The amended paragraph beginning on page 7, line 6 and ending on page 8, line 5:

A more complete understanding of the system and method of the present invention may be obtained by reference to the following Detailed Description when taken in conjunction with the accompanying Drawings wherein:

Figures 1A and 1B are circuit schematics of conventional 1T1C and 2T2C ferroelectric memory cells, respectively;

Figure 2 illustrates a conventional timing diagram for the read and restore operation of a ferroelectric memory cell;

Figure 3 illustrates the polarization characteristics of a ferroelectric memory cell operating under normal conditions and degraded conditions;

Figure 4 is a block diagram of a memory device according to an embodiment of the present invention;

Figure 5 is a test circuit for the memory device of Figure 4;

Figure 6 is an alternative embodiment of a portion of the test circuit for the memory device of Figure 4;

Figure 7 is a calibration test circuit for the test circuit of Figure 5;

Figure 8 is a flow chart illustrating an operation of the calibration test circuit of Figure 7;

Figure 9 is a flow chart illustrating a test operation of the memory device of Figure 4; and

Figure 10 is a block diagram of an apparatus incorporating the memory device of Figure 4.

After the paragraph beginning on page 20, line 1 and ending on page 20, line 10, the following new paragraph:

Referring to Figure 10, memory device 1 may form part of an apparatus including a processing unit having an address port connected to an address input port of memory device 1 and a data port connected to a data port of memory device 1.